

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: Akira MATSUDA et al.

Group Art Unit: 1775

Serial Number: 10/719,020

Examiner: Robert R. Koehler

Filed: November 24, 2003

P.T.O. Confirmation No.:

9168

PLATING BATH FOR FORMING THIN RESISTANCE LAYER, METHOD OF For:

FORMATION OF RESISTANCE LAYER, CONDUCTIVE BASE WITH RESISTANCE LAYER, AND CIRCUIT BOARD MATERIAL WITH

RESISTANCE LAYER

Attorney Docket No.: 032130 Customer Number: 38834

DECLARATION UNDER 37 CFR §1.132

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

March 5, 2006

Sir:

I, Akira Matsuda, hereby declare and state that:

I am familiar with the contents of the United States Patent Application Serial No.

10/719,020, filed on November 24, 2003, claiming the priority of Japanese Patent Application No.

2002-341813 filed on November 26, 2002.

I am one of the inventors of the invention of the above-identified application.

I have studied the contents of the cited references.

2/23/06